REMARKS

This paper is filed in response to the office action mailed on November 2, 2004. Claims 1-4 have been amended; claims 5-8 and 10-11 are withdrawn.

In the office action, the restriction requirement is made final and therefore claims 5-8 and 10-11 are withdrawn.

The office action rejects claims 3 and 4 under 35 U.S.C. § 112, second paragraph as allegedly being indefinite. In response, claims 3 and 4 have been amended to traverse this rejection. Applicants respectfully submit that all claims are now in full compliance with 35 U.S.C. § 112.

Turning to the rejections based upon the prior art, the Patent Office rejects claims 1-3 and 9 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,166,405 ("Kuriyama") in view of applicants' admitted prior art ("AAPA"). In response, claim 1 has been amended to traverse this rejection.

Under MPEP §§ 2142 and 2143,

> [t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Citing, In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); *see also* MPEP § 2143-§ 2143.03 for decisions pertinent to each of these criteria.

Claim 1 recites the forming of a spacer block mask over the spacer insulation layer and over the photodiode doping region. Claim 1 then recites that the spacer insulation layer is removed except the portion covered by the spacer block mask to form a spacer on a sidewall of the transistor. Claim 1 then recites that the spacer block mask is then removed before forming a second mask on top of the portion of the spacer insulation layer that remains on top of the photodiode doping region. Then, the floating diffusion region is formed in the open area opposite the transfer transistor while the second mask and the portion of the spacer

insulation layer remain in place on top of the photodiode doping region. Neither Kuriyama nor the AAPA teach or suggest this method.

Specifically, Kuriyama teaches away from the formation of a floating diffusion region while any mask is in place. See Kuriyama at Figs. 2C and 2D. Kuriyama clearly states that the resist layer 17b is removed prior to the implantation. See column 8, lines 47-48. See also Fig. 4G and Fig. 6D at Kuriyama. Kuriyama states at column 10, lines 56-64 that the process of Fig. 4G of Kuriyama is carried out in the same manner as the process of Fig. 2D of Kuriyama. That is, the resist layer 37b is removed prior to the implantation which results in a diffusion region in an area opposite the transistor from the photo receiving portion. Fig. 8 of Kuriyama also teaches the removal of oxide layer 46b prior to n-type impurity ion implantation. Similarly, the AAPA (Figs. 1E-1G) teaches the blanket etching of the entire spacer layer 18.

As a result, neither Kuriyama nor the AAPA teach or suggest the use of masks and spacer insulation layers to protect the photodiode region during the creation of the floating diffusion region. Applicants respectfully submit that the neither Kuriyama device nor the AAPA device can perform as well as that of the claimed invention. Still further, the layer at issue in Kuriyama, 17b, is a photoresist layer and is not a mask layer and clearly serves a completely different purpose than the spacer block mask and second mask of amended claim 1.

Accordingly, applicants respectfully submit that Kuriyama does not come close to teaching or suggesting all of the limitations of amended claim 1 and, in fact, teaches away from numerous limitations of amended claim 1 and therefore the obviousness rejection of claims 1-3 and 9 as being unpatentable over Kuriyama is improper and should be withdrawn.

Finally, the office action rejects claim 4 under 35 U.S.C. § 103 as being unpatentable over Kuriyama in view of the AAPA and further in view of Microchip Fabrication (2000) (Van Zant). The deficiencies of Kuriyama and the AAPA are addressed above. Specifically, no combination of Kuriyama and the AAPA teaches or suggests the use of a spacer block mask and portions of a spacer insulation layer to protect the photodiode region during the formation of a floating diffusion region. In fact, Kuriyama and the AAPA teach away from this strategy.

Van Zant, on the other hand, is merely cited for the proposition that it teaches certain uses of a negative photoresist to create a mask. However, Van Zant is not directed toward the specifics of amended claim 1 and it teaches nothing about improving the quality of a buried photodiode and therefore cannot supplement the deficiencies of Kuriyama and the AAPA. Accordingly, because amended claim 1 is clearly allowable over any hypothetical combination of Kuriyama, the AAPA and Van Zant, amended claim 4 is allowable as well.

An early action indicating the allowability of claims 1-4 and 9 is earnestly solicited.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

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Respectfully submitted,

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Attachments

Serial No. 10/669,996 - Filed 9/24/03
Inventor: Ju-Il Lee
Title: "Methd for Manufacturing CMOS Image Sensor Using Spacer Etching . . . "
ANNOTATED SHEET (Figs. 2D-2F)

FIG. 2D

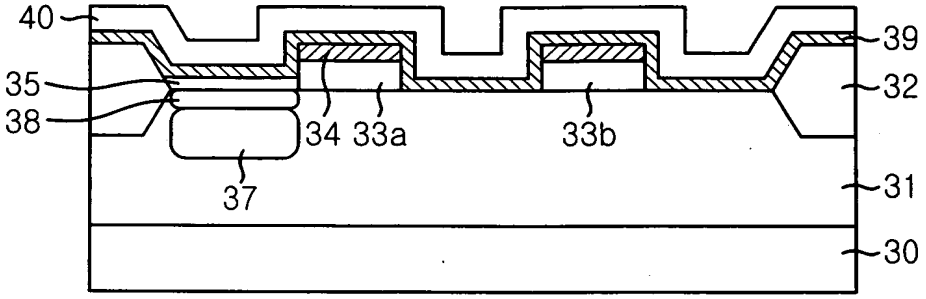

FIG. 2E

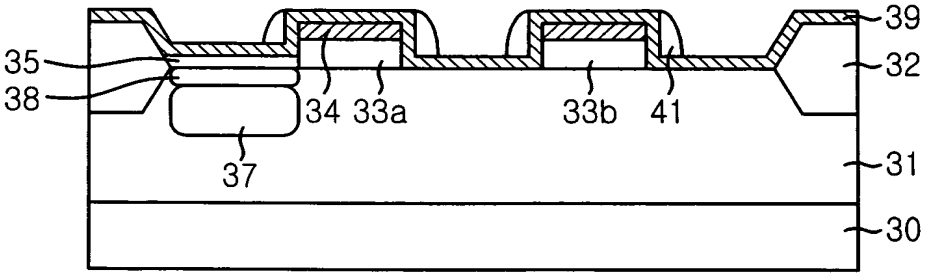

FIG. 2F